

**The University of Azad Jammu and Kashmir,**

**Muzaffarabad**

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**SR-Latch: -**

The SR (Set-Reset) latch is a 1-bit memory with SET and RESET inputs labelled as ‘S’ and ‘R,’ respectively. It is also a bistable device meaning it has 2 stable states namely 0 and 1. The SET input sets the device to produce output (Q) equal to 1, while the RESET input resets the device to produce output equal to 0.

**Inputs and Outputs**

* Inputs: **R (Reset)** and **S (Set)**
* Outputs: **Q** and **Q̅** (complement of Q)

**Basic Implementations**

There are **two common ways** to build an S-R latch:

**(A) Using NOR gates**

* Inputs are active **HIGH**.
* Circuit: Two cross-coupled NOR gates.

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| --- | --- | --- | --- | --- |
| **S** | **R** | **Qn+1** | **Qn+1** | **Note** |
| 0 | 0 | Qn | Qn | RETAIN |
| 0 | 1 | 1 | 0 | RESET |
| 1 | 0 | 0 | 1 | SET |
| 1 | 1 | 0 | 0 | FORBIDDEN |

*Table 2: Truth table of S R latch using NOR gates*

**(B) Using NAND gates**

* Inputs are active **LOW**.
* Circuit: Two cross-coupled NAND gates.

|  | | | | |
| --- | --- | --- | --- | --- |
| **S** | **R** | **Qn+1** | **Qn+1** | **Note** |
| 0 | 0 | 1 | 1 | FORBIDDEN |
| 0 | 1 | 1 | 0 | SET |
| 1 | 0 | 0 | 1 | RESET |
| 1 | 1 | Qn | Qn | RETAIN |

*Table 1: Truth table of S R latch using NAND gates*

This is how to understand the truth-table of SR latch using NOR gates:

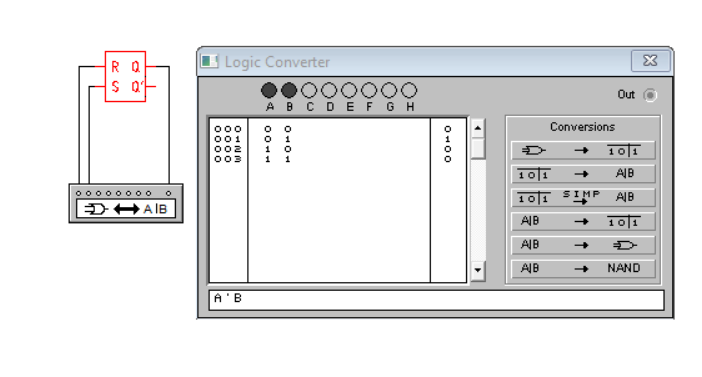
When both ‘S’ and ‘R’ are 0, the latch maintains its state. Whatever ‘Q’ was it stayed the same.

When ‘S’ is 0 and ‘R’ is 1, the latch resets, forcing ‘Q’ to be 0.

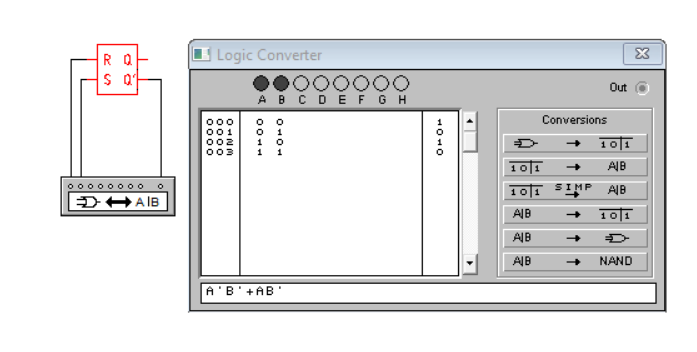
When ‘S’ is 1 and ‘R’ is 0, the latch sets, making ‘Q’=1.

When both ‘S’ and ‘R’ are 1, it’s an invalid or ambiguous condition (often referred to as a “forbidden” state in SR latch), resulting in both Q and Q being the same and 0.

**Truth table & Equation (Q)**



**Truth table & Equation (Q’)**

S